

SSC8167GS6A

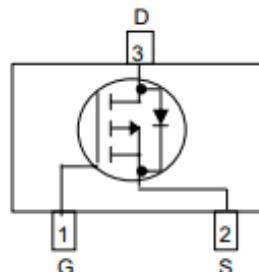
P-Channel Enhancement Mode MOSFET

➤ Features

VDS	VGS	RDS(on) Typ.	ID
-60V	$\pm 20V$	63m Ω @-10V	-5A
		70m Ω @-4V5	

➤ Pin configuration

Top view

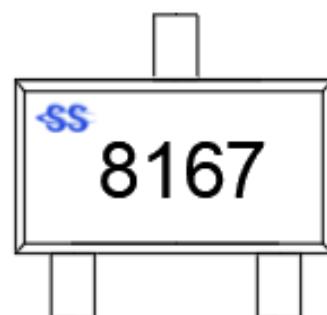


➤ Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits and low in-line power loss are needed in a very small outline surface mount package.



SOT23-3L



Marking

➤ Applications

- TFT panel power switch
- High side DC/DC Converter
- High side driver for brushless DC motor
- Portable DVD, DPF

➤ Ordering Information

Device	Package	Shipping
SSC8167GS6A	SOT23-3L	3000/Reel

➤ **Absolute Maximum Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-to-Source Voltage		-60	V
V_{GSS}	Gate-to-Source Voltage		± 20	V
I_D	Continuous Drain Current	TC=25°C	-5	A
		TC=100°C	-3	
I_{DSM}	Continuous Drain Current ^a	TA=25°C	-3.5	A
		TA=70°C	-2.4	
I_{DM}	Pulsed Drain Current ^b		-20	A
P_D	Power Dissipation ^c	TC=25°C	5	W
		TC=100°C	2	W
P_{DSM}	Power Dissipation ^a	TA=25°C	1.25	W
		TA=70°C	0.8	W
$T_J T_{STG}$	Storage and Operation junction temperature		-55 to 150	°C

➤ **Thermal Resistance Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		100	°C/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		24	

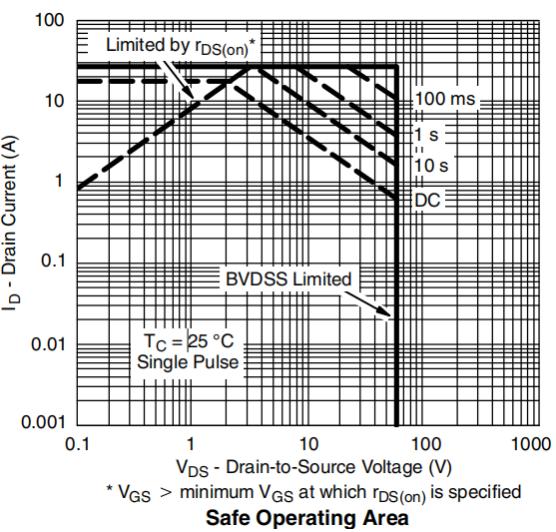
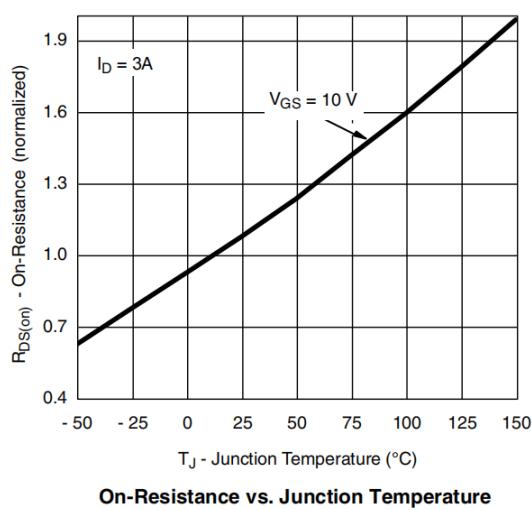
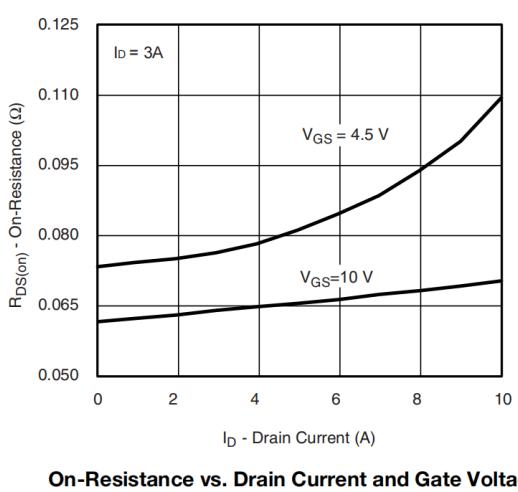
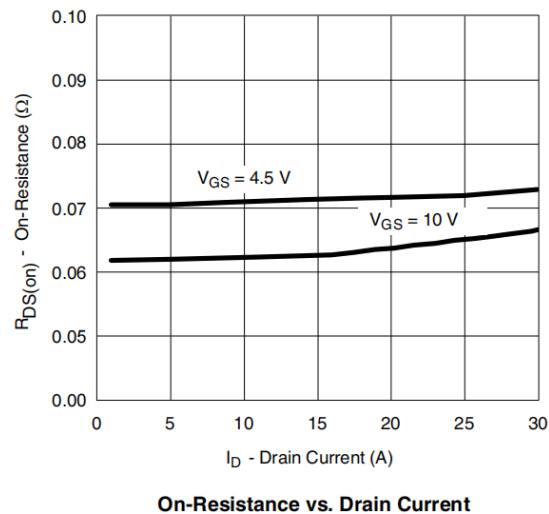
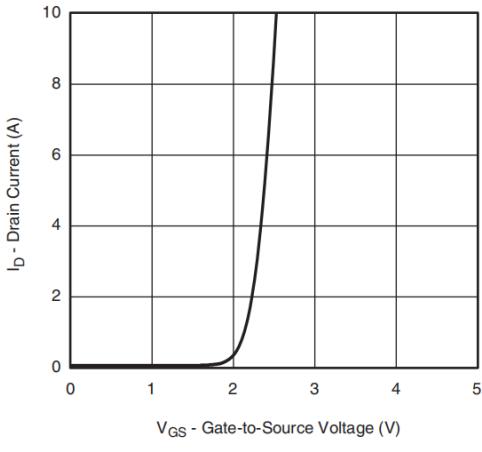
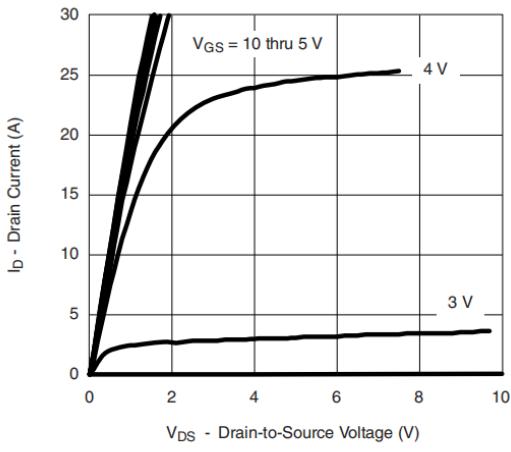
Note:

- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $TA=25^\circ\text{C}$.The value in any given application depends on the user specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_J(\text{MAX})=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

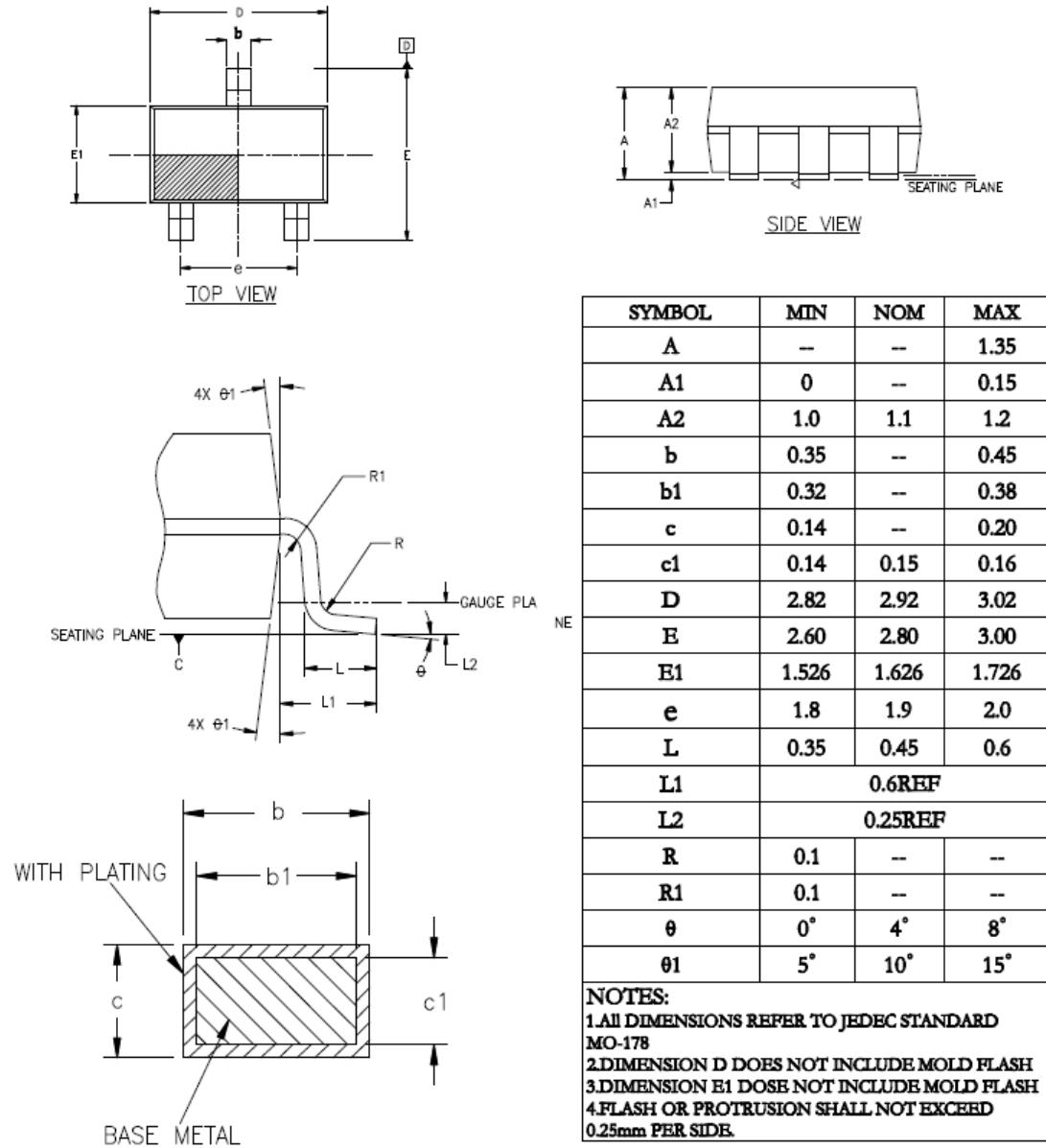
➤ Electronics Characteristics($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, ID=-250\mu A$	-60			V
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, ID=-250\mu A$	-1.0	-1.6	-2.5	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-10V, ID=-4A$		63	78	$m\Omega$
		$V_{GS}=-4.5V, ID=-2A$		70	90	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-60V, V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
V_{SD}	Forward Voltage	$V_{GS}=0V, IS=-3A$		-0.8	-1.3	V
C_{iss}	Input Capacitance	$V_{DS}=-30V, V_{GS}=0V, F=1MHz$		1592		pF
C_{oss}	Output Capacitance			63		
C_{rss}	Reverse Transfer Capacitance			47		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-10V, V_{DS}=-30V, RL=7.5\Omega, RG=3\Omega$		6.4		ns
T_r	Rise time			8.8		
$T_{D(OFF)}$	Turn-off delay time			95		
T_f	Fall time			34		
Q_G	Total Gate Charge	$V_{GS}=-10V, V_{DS}=-30V, ID=-4A$		27		nC
Q_{GS}	Gate to Source Charge			4.4		
Q_{GD}	Gate to Drain Charge			3.2		
T_{rr}	Diode Recovery Time	$IF=-4A, di/dt=100A/us$		22		ns
Q_{rr}	Diode Recovery Charge	$IF=-4A, di/dt=100A/us$		14		nC

➤ **Typical Characteristics**($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information



SOT23-3L



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