

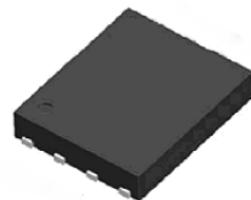
SSC8429GN6

P-Channel Enhancement Mode MOSFET

➤ Features

V _{DS}	V _{GS}	R _{DSON} Typ.	I _D
-20V	±12V	4mΩ@-4V5	-90A
		6mΩ@-2V5	

➤ Pin configuration

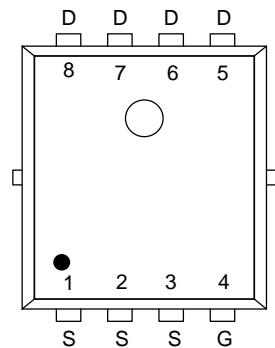


PDFN5X6-8L (Top View)

➤ Description

This SSC8429GN6 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

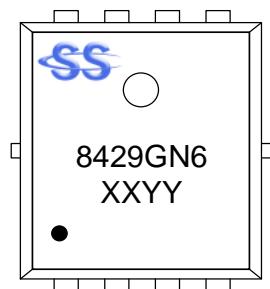
100% UIS + ΔVDS + R_g Tested!



Pin Configuration

➤ Applications

- Load Switch
- PWM Application
- Power Management



Marking

(XXYY: Internal Traceability Code)

➤ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^d	$T_C=25^\circ\text{C}$	-90
		$T_C=100^\circ\text{C}$	-48
I_{DSM}	Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	-27
		$T_A=70^\circ\text{C}$	-20
I_{DM}	Pulsed Drain Current ^b	-360	A
P_D	Power Dissipation ^c	$T_C=25^\circ\text{C}$	52
		$T_C=100^\circ\text{C}$	21
P_{DSM}	Power Dissipation ^a	$T_A=25^\circ\text{C}$	4.8
		$T_A=70^\circ\text{C}$	3
I_{AS}	Avalanche Current ^b L=0.5mH Single Pulse	-34	A
E_{AS}	Avalanche Energy ^b L=0.5mH Single Pulse	289	mJ
T_J	Operation junction temperature	-55~150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-55~150	

➤ Thermal Resistance Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	26	33	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	2.4	3.1	

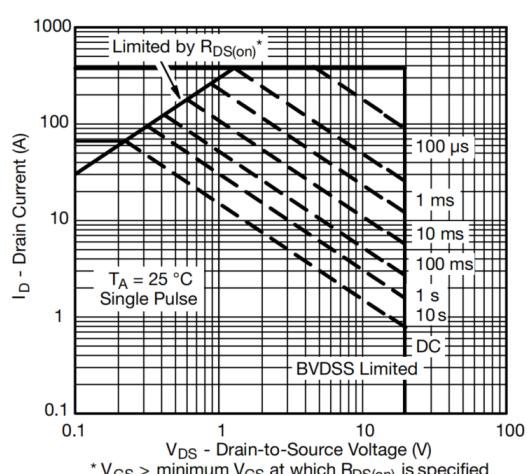
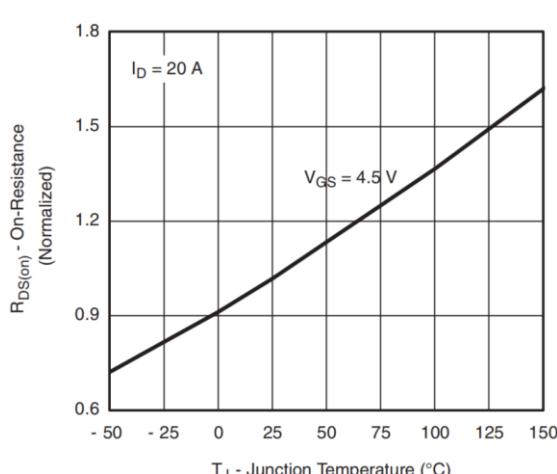
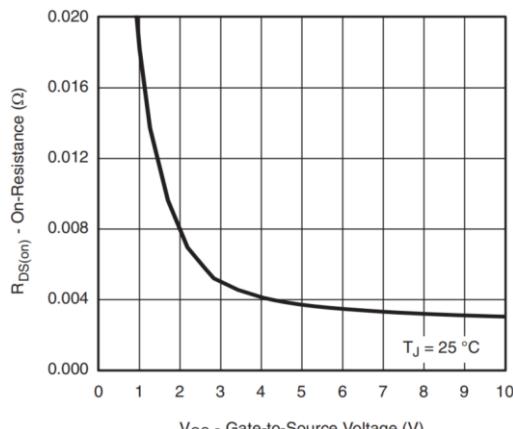
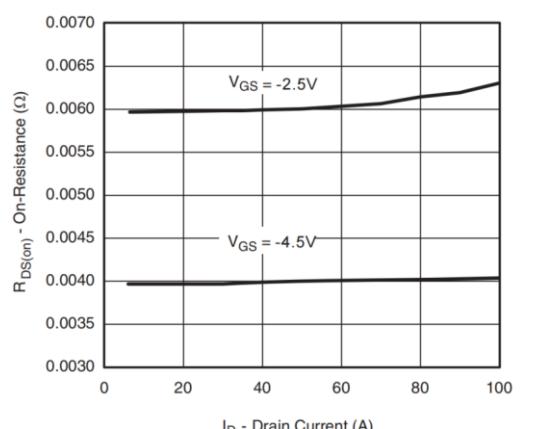
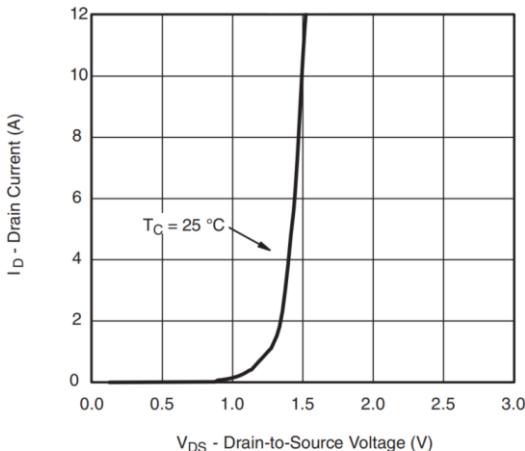
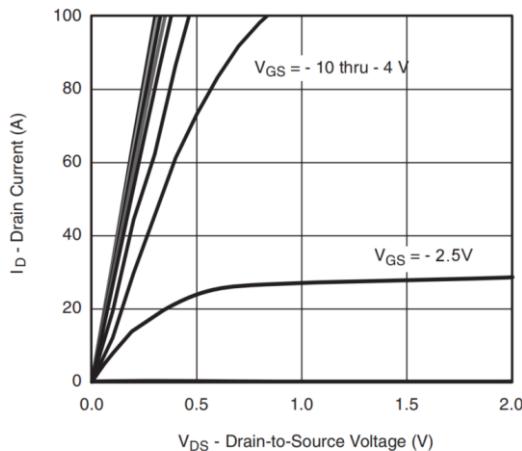
Note:

- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

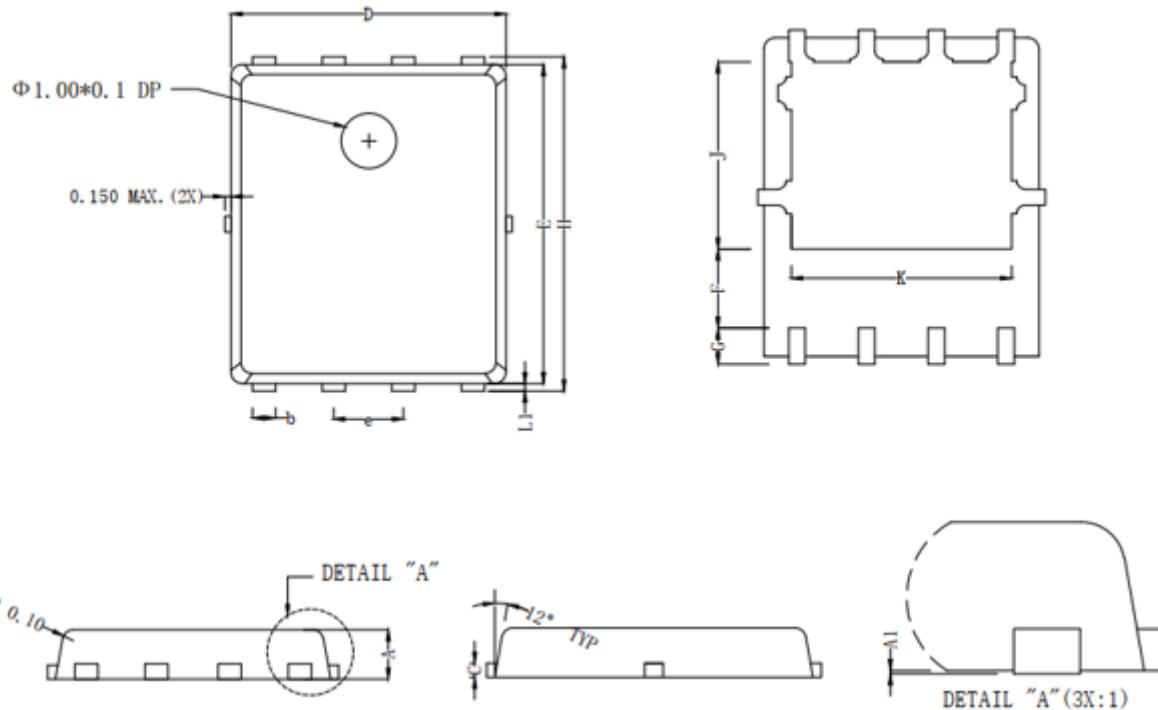
➤ Electrical Characteristics ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.5	-0.7	-1	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -15A$		4	7	$m\Omega$
		$V_{GS} = -2.5V, I_D = -10A$		6	9	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			1	μA
Gate-Source Leak Current	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$			± 100	nA
Transconductance	G_{FS}	$V_{DS} = -5V, I_D = -10A$		48		s
Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = -10A$		-0.7	-1.3	V
Gate Resistance	R_G	$V_{DS} = 0V, f = 1MHz$		1.8		Ω
Input Capacitance	C_{ISS}	$V_{DS} = -20V, V_{GS} = 0V,$ $f = 1MHz$		3712		pF
Output Capacitance	C_{OSS}			465		
Reverse Transfer Capacitance	C_{RSS}			368		
Total Gate Charge	Q_G	$V_{GS} = -4.5V, V_{DS} = -10V,$ $I_D = -20A$		25		nC
Gate to Source Charge	Q_{GS}			6.5		
Gate to Drain Charge	Q_{GD}			8.5		
Turn-on Delay Time	$T_{D(ON)}$	$V_{GS} = -4.5V, V_{DS} = -10V,$ $R_L = 2\Omega, R_G = 3\Omega$		18		ns
Rise Time	T_r			12		
Turn-off Delay Time	$T_{D(OFF)}$			36		
Fall Time	T_f			9		

➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.90	1.00	1.10
A1	0.00	0.03	0.05
b	0.25	0.03	0.35
c	0.254 REF		
D	4.80	4.90	5.00
F	1.35 REF		
E	5.65	5.75	5.85
e	1.27 BSC		
H	5.90	6.00	6.10
L1	0.10	0.13	0.16
G	0.55 REF		
K	4.00 REF		
J	3.45 REF		

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